

INTEGRATED CIRCUIT
WITH MULTIPROCESSOR ARCHITECTURE

BACKGROUND OF THE INVENTION

5 The present invention relates to an integrated circuit with multiprocessor architecture.

Microprocessors and DSPs (digital signal processors) are being widely used in many applications. Particularly, in the field of mobile communications under the recent remarkable 10 development, the information processability required is now several times as high as that of a known single processor and thus an architecture in which multiple processors share a memory, or a so-called multiprocessor architecture, has been widely adopted. On the other hand, as the design rule has 15 been reduced, an LSI (large-scale integrated circuit) including multiple processors and a memory that are integrated on a single chip, is now implementable.

FIG. 10 illustrates an example of a known multiprocessor structure. In this example, a first processor 500 and a second processor 510 both access a memory 520 through a memory controller 530 to carry out processing. The first processor 500 includes arithmetic and logic unit (ALU) 501, address output unit 502, clock supply unit 503 and reset control unit 504. Similarly, the second processor 510 includes arithmetic 25 and logic unit (ALU) 511, address output unit 512, clock sup-

ply unit 513 and reset control unit 514. The first and second processors 500 and 510 are coupled to the memory 520 through a data bus 540.

In this LSI, first, second and third reset signals RST1, RST2 and RST3 are asserted first, thereby resetting the first and second processors 500 and 510 and memory controller 530, respectively. In the first processor 500, when RST1 is asserted, the reset control unit 504 resets the units 501, 502 and 503 shown in FIG. 10 and units such as one (not shown) in charge of execution and control of instructions, for example. In the second processor 510, when RST2 is asserted, a similar reset operation is performed. The memory controller 530 is reset by RST3. A first clock signal CLK1 is supplied to the first processor 500. A second clock signal CLK2 is supplied to the second processor 510. A third clock signal CLK3 is supplied to the memory 520 and memory controller 530.

Next, when RST1, RST2 and RST3 are negated, the first and second processors 500 and 510, memory 520 and memory controller 530 start their predetermined operations. In this case, the first processor 500 operates synchronously with CLK1. The second processor 510 operates synchronously with CLK2. The memory 520 and memory controller 530 operate synchronously with CLK3. However, CLK1, CLK2 and CLK3 are out of phase with each other. Thus, the first and second processors 500 and 510, memory 520 and memory controller 530 oper-

ate asynchronously with each other.

Hereinafter, it will be described how the first processor 500 accesses the memory 520 after the reset operation has been performed.

5 FIG. 11 is a timing diagram illustrating a case where the first processor 500 reads data from the memory 520. The processor 500 synchronizes with CLK1, and at a time t_{51} , asserts a memory access signal MRW1 so as to indicate a read-state and outputs an address ADRS1. Since MRW1 is asserted, 10 the memory controller 530 selects ADRS1 as an address ADRS to be provided to the memory 520. However, MRW1 and ADRS1 are not synchronized with CLK3. Thus, the memory controller 530 provides a memory access signal MRW and an address ADRS that are synchronized with CLK3, to the memory 520 at a time t_{52} . 15 The memory 520 outputs data to the data bus 540 after a memory access time Δt_5 has passed. The arithmetic and logic unit 501 of the processor 500 synchronizes with CLK1 and receives the data from the data bus 540 at a time t_{53} .

FIG. 12 is a timing diagram illustrating a case where 20 the processor 500 writes data on the memory 520. The processor 500 synchronizes with CLK1, and at a time t_{54} , asserts MRW1 so as to indicate a write-state and outputs ADRS1 and data to the memory controller 530 and the data bus 540, respectively. Since MRW1 is asserted, the memory controller 25 530 selects ADRS1 as an address ADRS to be provided to the

memory **520**. However, MRW1 and ADRS1 are not synchronized with CLK3. Thus, the memory controller **530** provides MRW and ADRS which are synchronized with CLK3, to the memory **520** at a time **t55**. The memory **520** receives the data from the data bus 5 **540** at a time **t56**.

Where the second processor **510** reads or writes data from/on the memory **520**, a memory access signal **MRW2** output from the second processor **510** is asserted. The memory controller **530** then selects an address **ADRS2** supplied from the 10 second processor **510** as an address **ADRS** to be provided to the memory **520**. In the other respects, the same operations are performed.

However, in the known structure, data are not transferred at a high speed between the first or second processor 15 **500** or **510** and the memory **520** due to the phase differences among CLK1, CLK2 and CLK3. For example, to access the memory **520**, the first processor **500** needs two cycles of CLK1 (from the time **t51** to the time **t53**) in the memory read transaction 20 shown in FIG. 11 and about three cycles of CLK1 (from the time **t54** to the time **t56**) in the memory write transaction shown in FIG. 12.

In addition, the first processor **500** includes the clock supply unit **503** and reset control unit **504** and the second processor **510** also includes the clock supply unit **513** and 25 reset control unit **514**. Thus, where the processors are inte-

grated on a single chip, the total chip area increases.

Further, RST1, RST2 and RST3 have to be asserted or negated synchronously with CLK1, CLK2 and CLK3, respectively. Thus, it has been difficult to design the input timing of the 5 reset signals.

SUMMARY OF THE INVENTION

A main object of the present invention is to speed up memory access performed by each processor in an integrated 10 circuit with a multiprocessor architecture including a built-in memory.

To achieve the object, the present invention has adopted a configuration in which a first processor, a second processor, a memory and a clock supply unit are integrated together 15 on a single chip. The first processor operates synchronously with a first internal clock signal. The second processor operates synchronously with a second internal clock signal. The memory operates synchronously with a third internal clock signal. The clock supply unit generates three clock signals, 20 which are in phase with each other, from an external clock signal and supplies those clock signals as the first, second and third internal clock signals.

This is to say, phase locking has been accomplished among the three internal clock signals so that the first and 25 second processors, and the memory can operate synchronously

with each other, thus allowing each of the processor to access the memory at a high speed. As a result, the integrated circuit can have its information processability increased drastically.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a configuration for an LSI in accordance with a first embodiment of the present invention.

10 FIG. 2 illustrates an exemplary configuration for the clock supply unit shown in FIG. 1.

FIG. 3 illustrates an exemplary configuration for the reset control unit shown in FIG. 1.

15 FIG. 4 illustrates an exemplary configuration for the memory controller shown in FIG. 1.

FIG. 5 is a timing diagram illustrating a case where a memory read is performed in the LSI shown in FIG. 1.

FIG. 6 is a timing diagram illustrating a case where a memory write is performed in the LSI shown in FIG. 1.

20 FIG. 7 illustrates a modified example of the reset control unit shown in FIG. 1.

FIG. 8 is a block diagram illustrating a configuration for an LSI in accordance with a second embodiment of the present invention.

25 FIG. 9 illustrates an exemplary configuration for the

clock supply unit shown in FIG. 8.

FIG. 10 is a block diagram illustrating an example of a known multiprocessor structure.

FIG. 11 is a timing diagram illustrating a case where a 5 memory read is performed in the known multiprocessor structure shown in FIG. 10.

FIG. 12 is a timing diagram illustrating a case where a memory write is performed in the known multiprocessor structure shown in FIG. 10.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings.

15 EMBODIMENT 1

FIG. 1 illustrates a configuration for an LSI in accordance with a first embodiment of the present invention. An LSI 100 shown in FIG. 1 includes first processor 110, second processor 120, memory 130, clock supply unit 140, and reset 20 control unit 150 that are integrated together on a single chip. The first processor 110 includes an arithmetic and logic unit (ALU) 111 and an address output unit 112, and operates synchronously with a first internal clock signal ICLK1. Similarly, the second processor 120 includes an arithmetic 25 and logic unit (ALU) 121 and an address output unit 122, and

operates synchronously with a second internal clock signal **ICLK2**. The first and second processors **110** and **120** are coupled to a memory **130** via a data bus **160**. The memory **130** includes a memory array **131** and a memory controller **132**, and 5 operates synchronously with a third internal clock signal **ICLK3**.

FIG. 2 illustrates an exemplary configuration for the clock supply unit **140**. The clock supply unit **140** shown in FIG. 2 generates three clock signals, which are in phase with 10 each other, from an external clock signal **ECLK** and supplies those clock signals as the internal clock signals **ICLK1**, **ICLK2** and **ICLK3**. The clock supply unit **140** includes a PLL (phase-locked loop) **141** and three delay adjusting cells **142**, **143** and **144**. The PLL **141** receives the external clock signal 15 **ECLK** and outputs an intermediate clock signal **ICLK0**. The delay adjusting cells **142**, **143** and **144** adjust respective delays in **ICLK1**, **ICLK2** and **ICLK3** so that **ICLK1**, **ICLK2** and **ICLK3** are in phase with each other.

FIG. 3 illustrates an exemplary configuration for the 20 reset control unit **150**. The reset control unit **150** shown in FIG. 3 receives first, second and third external reset signals **ERES1**, **ERES2** and **ERES3** and supplies first, second and third internal reset signals **IRES1**, **IRES2** and **IRES3**. The first internal reset signal **IRES1** resets the memory **130** and clock supply unit **140**. The second internal reset signal **IRES2** resets 25

the first processor 110. The third internal reset signal **IRES3** resets the second processor 120. The reset control unit 150 includes an inverter 151 and two NOR gates 152 and 153. In the reset control unit 150, when **ERES1** is asserted (positive logic), **IRES1**, **IRES2** and **IRES3** are all asserted (negative logic). In this case, **ERES2** and **ERES3** may be in any logical state. If **ERES2** is asserted while **ERES1** is negated, only **IRES2** is asserted. If **ERES3** is asserted while **ERES1** is negated, only **IRES3** is asserted.

FIG. 4 illustrates an exemplary configuration for the memory controller 132. The memory controller 132 shown in FIG. 4 includes an OR gate 133 and a multiplexer 134, and receives first memory access signal **MRW1**, first address **ADRS1**, second memory access signal **MRW2** and second address **ADRS2**. The first memory access signal **MRW1** and first address **ADRS1** are output from the address output unit 112 of the first processor 110. The second memory access signal **MRW2** and second address **ADRS2** are output from the address output unit 122 of the second processor 120. When **MRW1** is asserted, the memory controller 132 selects and supplies **ADRS1** to the memory array 131. When **MRW2** is asserted, the memory controller 132 selects and supplies **ADRS2** to the memory array 131. **MRW** and **ADRS** are a memory access signal and an address, respectively, both of which are supplied to the memory array 131.

To reset the whole LSI 100 shown in FIG. 1, **ERES1** is as-

serted, thereby asserting all of the internal reset signals IRES1, IRES2 and IRES3. In this manner, all of the first and second processors 110 and 120, memory 130 and clock supply unit 140 are reset at the same time. Then, an external clock 5 signal ECLK is provided to the LSI 100.

Next, when ERES1 is negated, the first and second processors 110 and 120, memory 130 and clock supply unit 140 start their predetermined operations. In this case, the clock supply unit 140 supplies ICLK1, ICLK2 and ICLK3 which are in 10 phase with each other. Thus, the first and second processors 110 and 120 and memory 130 operate synchronously with each other.

Hereinafter, it will be described how the first processor 110 accesses the memory 130 after the reset operation has been 15 performed.

FIG. 5 is a timing diagram illustrating a case where the processor 110 reads data from the memory 130. At a time t_{11} , the processor 110 asserts MRW1 so as to indicate a read-state and outputs ADRS1. Since MRW1 is asserted, the memory controller 132 selects ADRS1 by the multiplexer 134, and 20 provides MRW and ADRS to the memory array 131 at the time t_{11} . The memory array 131 outputs data to the data bus 160 after a memory access time Δt_1 has passed. The arithmetic and logic unit (ALU) 111 of the processor 110 receives the data from 25 the data bus 160 at a time t_{12} and completes computations be-

fore a time t_{13} . This is to say, the processor **110** can complete the memory read in one cycle of ICLK1 (from the time t_{11} to the time t_{12}).

FIG. 6 is a timing diagram illustrating a case where the 5 processor **110** writes data on the memory **130**. At a time t_{14} , the processor **110** asserts MRW1 so as to indicate a write-state and outputs ADRS1 and data to the memory controller **132** and the data bus **160**, respectively. Since MRW1 is asserted, the memory controller **132** selects ADRS1 by the multiplexer 10 **134**, and supplies MRW and ADRS to the memory array **131** at the time t_{14} . The memory array **131** receives the data from the data bus **160** at a time t_{15} . This is to say, the processor **110** can complete the memory write in one cycle of ICLK1 (from the time t_{14} to the time t_{15}).

15 Where the second processor **120** reads or writes data from/on the memory **130**, MRW2 is asserted and the memory controller **132** selects ADRS2. In the other respects, the same operations are performed.

Where one of the processors **110** and **120** has completed 20 its processing or where it is needed to have one of the processors **110** and **120** restart its processing from the beginning, ERES2 or ERES3 may be asserted. For example, where the second processor **120** has completed its processing, ERES3 may be asserted. In this case, since the reset control unit **150** asserts only IRES3, only the second processor **120** is reset.

This is to say, the first processor 110, memory 130 and clock supply unit 140 continue their operations without being suspended.

As described above, according to this embodiment, the 5 clock supply unit 140 supplies ICLK1, ICLK2 and ICLK3 that are in phase with each other. The first and second processors 110 and 120 and memory 130 operate synchronously with ICLK1, ICLK2 and ICLK3, respectively. Thus, the memory controller 132 needs no specially provided circuit for the synchronization and the processors 110 and 120 can access the 10 memory 130 at a high speed. Also, the LSI 100 includes only one built-in clock supply unit 140 and one built-in reset control unit 150. Thus, the total chip area can be reduced 15 drastically as compared to the example shown in FIG. 10, in which each of the processors includes these units. In addition, ERES1, ERES2 and ERES3 may be provided to the LSI 100 by taking only the phase of the single external clock signal ECLK into account. Thus, it will be easier to design the input timing of the external reset signals.

20 FIG. 7 illustrates a modified example of the reset control unit 150. The reset control unit 150 shown in FIG. 7 includes two OR gates 201 and 202 and first, second and third flip-flops (FF) 203, 204 and 205. The first FF 203, which is used to supply IRES1, is connected to ICLK1. The second FF 25 204, which is used to supply IRES2, is connected to ICLK2.

The third FF 205, which is used to supply IRES3, is connected to ICLK3. In the reset control unit 150, when ERES1 is asserted (positive logic), IRES1, IRES2 and IRES3 are all asserted (negative logic). In addition, IRES1, IRES2 and IRES3 5 can be negated at the same time by ICLK1, ICLK2 and ICLK3 that are in phase with each other. If ERES2 is asserted while ERES1 is negated, only IRES2 is asserted. If ERES3 is asserted while ERES1 is negated, only IRES3 is asserted.

10 EMBODIMENT 2

FIG. 8 illustrates a configuration for an LSI in accordance with a second embodiment of the present invention. The LSI 300 shown in FIG. 8 differs from the LSI 100 of the first embodiment in that a clock supply unit 340 receives a first 15 terminating signal TERM1 and a second terminating signal TERM2.

FIG. 9 illustrates an exemplary configuration for the clock supply unit 340. The clock supply unit 340 shown in FIG. 9 is basically similar to the clock supply unit 140 shown in FIG. 2, i.e., generates three clock signals, which 20 are in phase with each other, from an external clock signal ECLK and supplies those clock signals as internal clock signals ICLK1, ICKL2 and ICLK3. The clock supply unit 340 includes an AND gate 341, a PLL 342, two OR gates 343 and 344, 25 and three delay adjusting cells 345, 346 and 347. The PLL

342 receives the external clock signal **ECLK** and outputs an intermediate clock signal **ICLK0**. The delay adjusting cells 345, 346 and 347 adjust respective delays in ICKL1, ICLK2 and ICLK3 so that ICKL1, ICLK2 are ICLK3 are in phase with each 5 other. Besides, when only TERM1 is asserted (positive logic), the OR gate 343 masks ICLK0. As a result, only the supply of ICLK1 is stopped. Also, when only TERM2 is asserted (positive logic), the OR gate 344 masks ICLK0. As a result, only the supply of ICLK2 is stopped. Moreover, where TERM1 and 10 TERM2 are asserted at the same time, an output **TERM** from the AND gate 341 is asserted and the PLL 342 stops supplying ICLK0. As a result, the supply of ICLK1, ICLK2 and ICLK3 is all stopped.

According to this embodiment, where at least one of the 15 processors 110 and 120 has completed its processing, any of the internal clock signals **ICLK1**, **ICLK2** and **ICLK3** will be terminated when unnecessary. Thus, power dissipation of the LSI 300 can be reduced. For example, where the second processor 120 has completed its processing, TERM2 is asserted. 20 Then, the clock supply unit 340 responds by stopping the supply of ICLK2. In this case, the supply of ICLK1 and ICLK3 is not stopped, thus allowing the first processor 110 to keep accessing the memory 130 and also continue its processing without being suspended.

25 In the foregoing embodiments, the LSIs 100 and 300, each

of which has two built-in processors and a built-in memory, have been described. However, the present invention may also be applicable to an LSI including three or more processors. In that case, the memory controller 132 may receive and select 5 three or more pairs of a memory access signal and an address. Also where an LSI includes two or more memory arrays, a unit which is equivalent to the memory controller 132 may be connected to each of the memory arrays.